Session 11 Overview

RF Building Blocks and PLLs

Chair: Bram Nauta, University of Twente, Enschede, The Netherlands

Associate Chair: Marc Tiebout, Infineon, Munich, Germany

RFIC design is a broad, fascinating, and complex topic. Already for many years researchers and designers from academia and industry have invented and proposed new or optimized circuits in silicon technologies. These RF circuits find their way to customers in existing and upcoming applications such as TV, cellular, WLAN, UWB, and radar applications. The ten presentations in this session document recent advances in RF solid-state circuits. The session covers the above mentioned applications in frequencies ranging from 90MHz up to 85GHz through LNA and PA blocks as well as through clock generation issues ranging from small VCO circuits to complete PLLs.

The session starts with an agile auto-tuning synthesizer architecture. The synthesizer achieves a low-power operation of 18mW and wide-tuning range from 90 to 770MHz. It includes a divide-by-3.5 circuit.

In Paper 11.2, differential CMOS LC-tank VCOs with single and double switch pairs are compared. A 0.3µm CMOS VCO is described that operates from 2.15 to 2.35GHz and achieves a record performance with a phase noise of -143.9dBc/Hz @3MHz drawing 4mA from a 2.5V supply.

Two quadrature VCOs are presented in papers 11.3 and 11.4. Paper 11.3 presents a phase-noise reduction technique in quadrature VCOs. The technique shapes the transistor's injected thermal noise and provides a phase-to-amplitude noise-conversion mechanism. The experimental designs are centered at 5.1 and 5.3GHz with phase noise of -132.6dBc/Hz and -134.4dBc/Hz at 1MHz offset, respectively. The 5mW low-power quadrature VCO of Paper 11.4 features a high frequency of 17GHz, low-voltage operation using a 1V supply, and a low phase noise of -110dBc/Hz at 1MHz offset.

The session continues with two CMOS broadband LNA designs. Paper 11.5 presents a 5GHz broadband LNA in a 90nm CMOS technology with an area of 0.025mm^2 that achieves 25dB gain, 2dB NF, -14dBm IIP3, and -13dB S_{11}. In Paper 11.6, a CMOS LNA for UWB based on a method that uses Miller effect for input matching is presented. The technique requires only one extra inductor at the gate besides the source-degeneration inductor to achieve wideband matching and improved noise figure.

A fast-settling PLL frequency synthesizer with frequency presetting is presented in Paper 11.7. The 0.4mm^2 chip is implemented in a 0.35µm CMOS process. The measured results demonstrate that the settling time is less than 10µs.

Next, two power amplifier designs are proposed. A 2-D propagation medium compatible with IC processes is introduced in Paper 11.8 to design a broadband power combiner, called "funnel". A 4-to-1 combiner based on this concept demonstrates a wideband power amplifier at 85GHz in a 0.13µm SiGe BiCMOS process. In Paper 11.9, a single-chip 0.18µm CMOS linear PA for WLAN applications is proposed. All components, including the input balun and output transformer are integrated and no off-chip components are required.

In the last paper of this session, Paper 11.10, a CMOS low-power digitally controlled oscillator for UMTS is presented. Drawing 3.2mA from a 2.5V supply, it reaches a phase-noise target of -118dBc/Hz at 1MHz offset. A tuning range from 3.45 to 4.45GHz with a maximum frequency step of 200kHz is achieved by using a combination of binary-weighted and thermometer-coded switchable capacitors..

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11.1 An 18mW 90-to-770MHz Synthesizer with Agile Auto-Tuning for Digital TV Tuners **8:30 AM**
M. Marutani, Fujitsu, Kawasaki, Japan

An 18mW 90-to-770MHz I/Q synthesizer is fabricated in a 1.2V 0.11µm CMOS process. The architecture is optimized to achieve low power and wide tuning range. A divide-by-3.5 7b VCO with an agile auto-tuning block is included. Phase noise is <-100dBc/Hz at 100kHz offset.

11.2 A 2.3GHz LC-Tank CMOS VCO with Optimal Phase Noise Performance **9:00 AM**
P. Andreani, Technical University of Denmark, Lyngby, Denmark

The phase-noise theory and design of a differential CMOS LC-tank VCO with double switch pair is presented. A formula for the minimum achievable phase noise in the $1/f^2$ region is derived. The 2.15 to 2.35GHz 0.3µm CMOS VCO has a phase noise of -143.9dBc/Hz at 3MHz offset and draws 4mA from a 2.5V supply.

11.3 A Phase-Noise Reduction Technique for Quadrature LC-VCO with Phase-to-Amplitude Noise Conversion **9:30 AM**
C-W. Yao, University of California, Los Angeles, CA

A phase-noise reduction technique for quadrature VCOs reduces and shapes the transistor thermal noise injected into the system, and also provides a phase-to-amplitude noise conversion mechanism to further reduce phase noise. Two experimental designs provide 17% and 1% tuning ranges centered at 5.1GHz and 5.3GHz with phase noise of -132.6dBc/Hz and -134.4dBc/Hz at a 1MHz offset, respectively.

11.4 A 1V 17GHz 5mW CMOS QVCO Based on Transformer Coupling **9:45 AM**
W. Ng, The Hong Kong University of Science and Technology, Hong Kong, China

A 1V 17GHz 5mW QVCO is designed using transformer coupling for high frequency, low voltage and low phase noise. Implemented in 0.18µm CMOS, the 0.37mm^2 chip achieves a tuning range of 16.5% at 17GHz, a phase noise of -110dBc/Hz at 1MHz offset while using 5mA from a 1V supply, resulting in a FOM of 187.6dB.

11.5 A 5GHz Resistive-Feedback CMOS LNA for Low-Cost Multi-Standard Applications **10:15 AM**
J-H. Zhan, Intel, Hillsboro, OR

A 5GHz broadband LNA achieves 25dB gain, 2dB NF, -14dBm IIP3 and -13dB S11 while drawing 15.5mA from a 2.7V supply. The circuit is fabricated in an RF-enhanced 90nm CMOS technology. The active die area is 0.025mm^2.

11.6 A 3 to 5GHz CMOS UWB LNA with Input Matching Using Miller Effect **10:30 AM**
D. Ha, Virginia Institute of Technology, Blacksburg, VA

A UWB CMOS LNA uses the Miller effect with one additional inductor to achieve a broadband input match. The LNA has a power gain>15dB, S_{11}<-10.5dB, S_{22}<-13.1dB and NF<2.3dB over the 3 to 5GHz range. It is fabricated in 0.18µm CMOS and draws 6.4mA from a 1.8V supply.

11.7 A Fast-Settling PLL Frequency Synthesizer with Direct Frequency Presetting **10:45 AM**
X. Kuang, Chinese Academy of Sciences, Beijing, China

A PLL frequency synthesizer with frequency presetting is implemented in a 0.35µm CMOS process and occupies 0.4mm^2. The output frequency is between 560 and 820MHz, the supply is 3.3V, the measured settling time is <10µs and the phase noise is -85dBc/Hz at 10kHz offset. The synthesizer can automatically compensate for frequency variation with temperature.

11.8 An Electrical Funnel: a Broadband Signal Combining Method **11:15 AM**
E. Afshari, California Institute of Technology, Pasadena, CA

A non-uniform 2D propagation medium is compatible with modern IC processes and is used to produce a 4-to-1 broadband power combiner called an electrical funnel. The combiner is used in a wideband power amplifier in a 0.13µm SiGe BiCMOS process and yields 125mW peak output power at 85GHz with a 24GHz 3dB bandwidth.

11.9 A Single-Chip CMOS Power Amplifier for 2.4 GHz WLAN **11:45 AM**
J. Kang, Pohang University of Science and Technology, Pohang, Korea

A single-chip linear CMOS PA for OFDM WLAN applications adopts a fully differential topology with transformer-type output matching and operates from a 3.3V supply. All of the components, including the input balun and output transformer, are integrated on a single 0.18µm CMOS die and no off-chip component is required.

11.10 A UMTS-Compliant Fully Digitally Controlled Oscillator with 100MHz Fine Tuning Range in 0.13µm CMOS **12:00 PM**
T. Pittorino, University of Linz, Linz, Austria

A 0.13µm CMOS fully digitally controlled oscillator is presented. Running at 2GHz, it draws 3.2mA from a 2.5V supply and has a phase noise of -118dBc/Hz at 1MHz offset, as required for UMTS oscillators. A tuning range from 3.45 to 4.45GHz is achieved by using binary-weighted and thermometer-coded switchable capacitors, which allow a maximum frequency step of 200kHz.